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EXAMINER	
CAO, PHAT X	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/722,218	Applicant(s) CHENG ET AL.	
	Examiner Phat X. Cao	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 28 August 2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-49 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-49 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Request for Continued Examination filed on 8/28/06 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 8-12, and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Ouyang et al (US. 2005/0093021).

Regarding claims 1 and 44, Ouyang (Fig. 4B) discloses a method of manufacturing a semiconductor device, comprising: forming an isolation region 54 located in a substrate; forming an NMOS device located partially over a surface of the substrate 40'; and forming a PMOS device isolated from the NMOS device by the isolation region 54 and located partially over the surface 40 (par. [0040]); wherein a first one of the NMOS and PMOS devices includes the PMOS device having first source/drain regions 10 recessed within the surface 40 (par. [0040], lines 8-13); and wherein a second one of the NMOS and PMOS devices includes the NMOS device having second source/drain regions 70 substantially coplanar with the surface 40'.

Regarding claims 5 and 12, Ouyang (Fig. 4B) further discloses that the set of PMOS source/drain regions comprise strained source/drain regions 10 of SiGe (par. [0027], lines 9-17 and par. [0028]).

Regarding claims 8-9, Ouyang further discloses that the substrate has a {110} or {100} crystal orientation (par. [0029]).

Regarding claims 11 and 12, Ouyang also discloses that the substrate is a bulk silicon substrate or a silicon-on-insulator substrate (SOI) (par. [0033]).

3. Claims 1, 5-7, 8-9, 11-12, 15, 38-39, 42-43, and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Bohr et al (US. 2004/0262683).

Regarding claims 1, 5-7, 38-39, and 44, Bohr (fig. 6) discloses a semiconductor device, comprising: an isolation region 110 located in a substrate; an NMOS device 603 located partially over a surface of the substrate; and a PMOS device 604 isolated from the NMOS device 603 by the isolation region 110 and located partially over the surface; wherein a first one of the NMOS and PMOS devices includes first source/drain regions 470/480 recessed within the surface (see recesses 340 and 360 in Fig. 3) and comprising SiGe or SiC (par. [0024]); and wherein a second one of the NMOS and PMOS devices includes second source/drain regions 203 substantially coplanar with the surface and not comprising either of SiC and SiGe (par. [0020]. Lines 1-5).

Regarding claims 8-9, 11-12 and 42, Bohr's Fig. 6 further discloses that the substrate is a bulk silicon substrate having a <110> or <100> crystal orientation (par. [0027], last 5 lines), and the first source/drain regions 470/480 comprises strained source/drain regions at strain 494 (par. [0026]).

Regarding claims 15 and 43, Bohr also discloses an etch stop layer 663/664 (par. [0039], lines 1-6) located over the NMOS and PMOS devices (Fig. 6) and imparting a first stress in the first source/drain regions 470/480 and a second stress in the second source/drain regions 203, wherein the first and second stresses are substantially different in magnitude (par. [0039]).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 16-17, 24, 28, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Dawson et al (US. 5,963,803).

Regarding claims 16-17 and 28, Dawson (Fig. 1L) discloses a semiconductor device, comprising: an isolation region 110 located in a substrate; an NMOS device located partially over a surface of the substrate; and a PMOS device isolated from the NMOS device by the isolation region 110 and located from the NMOS device by the isolation region 110 and located partially over the surface; wherein a first one of the NMOS and PMOS devices includes: first source/drain regions 150/152 located at least partially in the substrate, a first gate 126 interposing the first source/drain regions and having a first gate height over the surface, and first spacers 144 on opposing sides of the first gate 126 and each extending from the first gate 126 to a first width; wherein a second one of the NMOS and PMOS devices includes: second source/drain regions 160/162 located at least partially in the substrate, a second gate 122 interposing the

second source/drain regions and having a second gate height over the surface, and second spacers 146 on opposing sides of the second gate 122 and each extending from the second gate to a second width; wherein the first and second gate heights 126 and 122 are substantially different (column 7, lines 4-6), and the first and second widths of spacers 144 and 146 are substantially different (column 7, lines 4-6). It is noted that the substantial differences between the first and second gate heights and between the first and second spacer widths would indirectly cause a substantially difference in magnitudes of first and second stresses in the first and second source/drain regions because the first and second gates and the first and second spacers are formed indirectly on the first and second source/drain regions.

Regarding claims 24 and 35, Dawson's Fig. 1L also discloses that the substrate 102 is a bulk silicon substrate (column 4, lines 61-62).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-4, 13-14, 16-18, 21-26, 28-29, 32-36, and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al in view of Dawson et al (US. 5,963,803).

Regarding claims 2, 16 and 45, Ouyang's Fig. 4B also discloses that the

magnitudes of stresses in the first and second source/drain regions are different, the difference in magnitudes of stresses are caused by the difference in structures of the first and second source/drain regions of the NMOS and PMOS devices (par. [0027]).

Ouyang does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claims 3-4, 17, 28 and 46, as discussed above, Ouyang's Fig. 4B substantially reads on the invention as claimed, except it does not disclose that the spacers 51 formed on opposing sides of the PMOS have a width greater than a width of the spacers 51 formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the spacers on opposing sides of the PMOS gate having a width greater than a width of the spacers on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the

source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

Regarding claims 13-14, 18, 25-26, 29, and 36, Ouyang's Fig. 4B further discloses that the set of PMOS source/drain regions comprise strained source/drain regions 10 of SiGe (par. [0027], lines 9-17 and par. [0028]).

Regarding claims 21-22, 23-24, and 32-35, Ouyang also discloses that the substrate has a {110} or {100} crystal orientation (par. [0029]) and the substrate is a bulk silicon substrate or a silicon-on-insulator substrate (SOI) (par. [0033]).

8. Claims 6-7, 38-39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al as applied to claim 1 above, and further in view of Yeo et al (US. 2004/0173815).

Regarding claims 6-7 and 38, Ouyang's Fig. 4B discloses a semiconductor device, comprising: an isolation region 54 located in a substrate; an NMOS device located partially over a surface of the substrate 40'; and a PMOS device isolated from the NMOS device by the isolation region 54 and located partially over the surface 40; wherein the PMOS device includes first source/drain regions 10 located at least partially within the substrate 40 and comprising SiGe (par. [0040]); and wherein the NMOS device includes second source/drain regions 70 located at least partially within the substrate 40'.

Ouyang does not disclose that the NMOS source/drain regions 70 comprise SiC.

However, Yeo (Fig. 3B) teaches an NMOS device 3b having source/drain regions 304b/302b comprising silicon and lattice-mismatched zone 305b made of silicon-carbon alloy (SiC) (par. [0033]). Accordingly, it would have been obvious to modify the device of Ouyang by forming the NMOS device having source/drain regions comprising silicon and lattice-mismatched zone made of SiC because such lattice-mismatched zone of SiC would significantly enhance the electron mobility of the drive current in the strained channel region, as taught by Yeo (par. [0033], last 8 lines).

Regarding claims 39 and 42, Ouyang's Fig. 4B further discloses that the first source/drain regions 10 of the PMOS device are recessed within the surface (par. [0040]) and the second source/drain regions 70 of the NMOS device extend downward from the surface, and the set of the first source/drain regions 10 of PMOS device comprises strained source/drain regions (par. [0027], lines 9-17 and par. [0028]).

9. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Yeo et al as applied to claim 38 above, and further in view of Dawson et al (US. 5,963,803).

Regarding claim 40, Ouyang does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the PMOS gate having a height greater than a height of the NMOS gate because the

relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 41, Ouyang does not disclose that the spacer 51 formed on opposing sides of the PMOS gate has a width greater than a width of the spacer 51 formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the spacers on opposing sides of the PMOS gate having a width greater than a width of the spacers on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

10. Claims 19-20 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Dawson et al as applied to claim (16,28) above, and further in view of Yeo et al (US. 2004/0173815).

Ouyang does not disclose that the NMOS source/drain regions 70 comprises SiC.

However, Yeo (Fig. 3B) teaches an NMOS device 3b having source/drain regions 304b/302b comprising silicon and lattice-mismatched zone 305b made of silicon-carbon

alloy (SiC) (par. [0033]). Accordingly, it would have been obvious to modify the device of Ouyang by forming the NMOS device having source/drain regions comprising silicon and lattice-mismatched zone made of SiC because such lattice-mismatched zone of SiC would significantly enhance the electron mobility of the drive current in the strained channel region, as taught by Yeo (par. [0033], last 8 lines).

11. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al (US. 2005/0093021) in view of Okumura et al (US. 5,428,239).

Ouyang (Fig. 4B) discloses an integrated circuit device, comprising a CMOS including: an isolation region 54 located in a substrate; an NMOS device located partially over a surface of the substrate 40'; and a PMOS device isolated from the NMOS device by the isolation region 54 and located partially over the surface 40 (par. [0040]); wherein a first one of the NMOS and PMOS devices includes the PMOS device having first source/drain regions 10 recessed within the surface 40 (par. [0040], lines 8-13); and wherein a second one of the NMOS and PMOS devices includes the NMOS device having second source/drain regions 70 substantially coplanar with the surface 40'.

Ouyang does not disclose that the integrated circuit device comprising a plurality of CMOS devices.

However, Okumura (Fig. 1) teaches the forming of a memory integrated circuit device comprising a plurality of CMOS devices. Accordingly, it would have been obvious to modify the device of Ouyang by forming a plurality of CMOS devices in order to provide a DRAM device, as taught by Okumura (see abstract). It also would have

been obvious to provide a plurality of interconnects connecting ones of the plurality of CMOS devices because such interconnects connections are well known in the art for providing the electrical connections to the CMOS devices.

12. Claims 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Okumura et al as applied to claim 47 above, and further in view of Dawson et al (US. 5,963,803).

Regarding claim 48, Ouyang does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 49, Ouyang does not disclose that the spacer 51 formed on opposing sides of the PMOS gate has a width greater than a width of the spacer 51 formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the spacers on opposing sides of the PMOS gate having a width greater than a

width of the spacers on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

13. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al in view of Shimizu (IEEE).

Ouyang does not disclose an etch stop layer over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices.

However, Shimizu (Fig. 1) teaches the forming of an etch stop layer of SiN over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices (see first two pages). Accordingly, it would have been obvious to form over the NMOS and PMOS devices of Ouyang with the etch stop structure as set forth above in order to improve the drive currents for both NMOS and PMOS devices, as taught by Shimizu (see abstract).

14. Claims 27 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Dawson et al as applied to claim (16,28) above, and further in view of Shimizu et al (IEEE).

Ouyang does not disclose an etch stop layer over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices.

However, Shimizu (Fig. 1) teaches the forming of an etch stop layer of SiN over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices (see first two pages). Accordingly, it would have been obvious to form over the NMOS and PMOS devices of Ouyang with the etch stop structure as set forth above in order to improve the drive currents for both NMOS and PMOS devices, as taught by Shimizu (see abstract).

15. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Yeo et al as applied to claim 38 above, and further in view of Shimizu et al (IEEE).

Ouyang does not disclose an etch stop layer over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices.

However, Shimizu (Fig. 1) teaches the forming of an etch stop layer of SiN over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices (see first two pages). Accordingly, it would have been obvious to form over the NMOS and PMOS devices of Ouyang with the etch stop structure as set forth above in order to improve the drive currents for both NMOS and PMOS devices, as taught by Shimizu (see abstract).

16. Claims 18-20, 25-26, 29-31, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson et al (US. 5,963,803) in view of Yeo et al (US. 2004/0173815).

Dawson does not disclose that the first and second source/drain regions

comprises strained source/drain regions of SiGe or SiC.

However, Yeo teaches a PMOS device 3 a (Fig. 3a) having strained source/drain regions 304a/302a comprising lattice-mismatched zone 305a made of SiGe (par. [0031]), and an NMOS device 3b (Fig. 3B) having strained source/drain regions 304b/302b comprising lattice-mismatched zone 305b made of SiC (par. [0033]). Accordingly, it would have been obvious to modify the device of Dawson by forming the PMOS device 122 having strained source/drain regions comprising lattice-mismatched zone made of SiGe and the NMOS device 126 having strained source/drain regions comprising lattice-mismatched zone made of SiC because such strained source/drain regions would significantly enhance the hole mobility of the drive current in the strained channel region of the PMOS, and would significantly enhance the electron mobility of the drive current in the strained channel region of the NMOS, as taught by Yeo (par. [0031], last 8 lines, and par. [0033], last 8 lines).

17. Claims 2-4, 13-14, 16-22, 24-27, 28-33, 35-37, 40-41, and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al (US. 2004/0262683) in view of Dawson et al (US. 5,963,803).

Regarding claims 2, 16, 40 and 45, Bohr does not disclose the PMOS gate 604 having a height greater than a height of the NMOS gate 603.

However, Dawson (Fig. 1H) teaches a CMOS device comprising: a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the PMOS gate having a height greater than a height of he NMOS gate because the

relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claims 3-4, 17, 28, 41, and 46, as discussed above, Bohr's Fig. 6 substantially reads on the invention as claimed, except that it does not disclose that the spacers formed on opposing sides of the PMOS gate 604 have a width greater than a width of the spacers formed on opposing sides of the NMOS gate 603.

However, Dawson (Fig. 1H0 teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the spacers formed on opposing sides of the PMOS gate having a width greater than a width of the spacers formed on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

Regarding claims 13-14, 18-22, 24-26, 29-33, and 35-36, Bohr (fig. 6) further discloses that the substrate is a bulk silicon substrate having a <110> or <100> crystal orientation (par. [0027], last 5 lines), and the first source/drain regions 470/480 comprises strained source/drain regions made of SiGe or SiC (par. [0024]).

Regarding claims 27 and 37, Bohr also discloses an etch stop layer 663/664 (par. [0039], lines 1-6) located over the NMOS and PMOS devices (Fig. 6) and

imparting a first stress in the first source/drain regions 470/480 and a second stress in the second source/drain regions 203, wherein the first and second stresses are different in magnitude (par. [0039]).

18. Claims 10, 23, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al and Dawson et al as applied to claims (16, 28) above, and further in view of Biebl et al (US. 5,913,115).

Neither Bohr nor Dawson discloses that the substrate is a silicon-on-insulator substrate.

However, Biebl (Fig. 9) teaches the known feature of forming a PMOS 26 and an NMOS 28 on a surface of a bulk silicon substrate or on a surface of a silicon-on-insulator (SOI) substrate 21 (column 4, lines 45-47). Accordingly, it would have been obvious to modify the device of Bohr by forming the PMOS and NMOS transistors on an SOI substrate because such known SOI substrate would reduce the parasitic effects between the transistors and the substrate.

19. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al (US. 2004/0262683) in view of Wuu (US. 6,194,258).

Bohr (Fig. 6) discloses a plurality of CMOS semiconductor devices (par. [0012], lines 1-5) each including: an isolation region 110 located in a substrate; an NMOS device 603 located partially over a surface of the substrate; and a PMOS device 604 isolated from the NMOS device 603 by the isolation region 110 and located partially over the surface; wherein the PMOS device 604 includes first source/drain regions 470/480 recessed within the surface (see recesses 340/360 in Fig. 3); and wherein the

NMOS device 603 includes second source/drain regions 203 substantially coplanar with the surface.

Bohr does not specifically disclose a plurality of interconnects connecting to CMOS device.

However, Wuu (Fig. 8) teaches the known feature of connecting a plurality of interconnects 16/18 to CMOS device 70/80. Accordingly, it would have been obvious to provide a plurality of interconnects connecting one of the plurality of CMOS devices of Bohr because such interconnects connections are well known in the art for providing the electrical connections to the CMOS devices.

20. Claims 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al and Wuu as applied to claim 47 above, and further in view of Dawson et al (US. 5,963,803).

Regarding claim 48, Bohr's Fig. 6 does not disclose the PMOS gate 604 having a height greater than a height of the NMOS gate 603.

However, Dawson (Fig. 1H) teaches a CMOS device comprising: a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the PMOS gate having a height greater than a height of he NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 49, Bohr's Fig. 6 does not disclose that the spacers formed on opposing sides of the PMOS gate 604 have a width greater than a width of the spacers formed on opposing sides of the NMOS gate 603.

However, Dawson (Fig. 1H0 teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the spacers formed on opposing sides of the PMOS gate having a width greater than a width of the spacers formed on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

Response to Arguments

21. Regarding the rejections of claims as being unpatentable over Ouyang, Applicants assert that Ouyang is disqualified as a prior art because a signed Declaration from inventors is submitted to establish that the invention claimed in the application was reduced to practice prior to October 31, 2003, the filling date of the Ouyang reference. Applicants also assert in Declaration that "...A redacted copy of the TSMC invention Disclosure form is attached." However, there is no such copy of the invention Disclosure form in the application. Therefore, Applicants fail to provide the evidences to support that the invention as claimed was reduced to practice prior to the filling date of

the Ouyang reference (see M.P.E.P. 715.07). Thus, the rejections of claims as being unpatentable over Ouyang are maintained. Moreover, the new references are applied in the new ground of rejections.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
October 30, 2006

Cao
PHAT X. CAO
PRIMARY EXAMINER